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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,901	09/26/2003	Kazi Asaduzzaman	174/280	9181

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EXAMINER	
BROWN, MICHAEL J	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,901	ASADUZZAMAN ET AL.	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,21-30 and 32-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-30 and 32-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-13, 18-19, 21-30, and 32-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Co et al.(US Patent 5,631,587).

As to claim 1, Co et al. discloses circuitry(PPL 2, see Fig. 6) for providing a dynamically adjustable bandwidth(loop bandwidth, see column 4, line 20) comprising a phase frequency detector(phase detector 300, see Fig. 6) receiving as input a clock signal(signal line 30, see Fig. 6) and having a signal output(signal line 50, see Fig. 6), a charge pump(charge(current) pump 400, see Fig. 3) having a pump input(signal line 50, see Fig. 6) coupled to the signal output of the phase frequency detector and having a pump output(signal line 60, see Fig. 6), and a loop filter(loop filter 500, see Fig. 6) input coupled to the pump output of the charge pump and having a filter output(signal line 70, see Fig. 6). Co also discloses a voltage controlled oscillator(Variable (Voltage Controlled) Oscillator 600, see Fig. 6) having an oscillator input(signal line 70, see Fig. 6) coupled to the filter output of the loop filter and having an oscillator output(signal line 20, see Fig. 6), a divider circuit(output frequency divider 200, see Fig. 6) having a

divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector, and control circuitry(phase-locked loop adjustment circuit 3, see Fig. 6) that receives as input at least one control signal(signal line 80, see Fig. 6) and is operative to dynamically adjust a setting in at least one of the charge pump, the loop filter, the voltage controlled oscillator, and the divider circuit while the circuitry is processing data(see column 6, lines 35-39).

As to claim 2, Co discloses the circuitry wherein the circuitry is clock data recovery circuitry(see column 6, lines 11-12).

As to claim 3, Co discloses the circuitry wherein the circuitry is phase locked loop circuitry(see column 6, lines 11-12).

As to claim 4, Co discloses the circuitry wherein the setting in the charge pump that can be dynamically adjusted is current(see column 6, lines 18-20).

As to claim 5, Co discloses the circuitry wherein the setting in the loop filter that can be dynamically adjusted is at least one of a resistor value(see column 6, lines 20-22).

As to claim 6, Co discloses the circuitry wherein the setting in the voltage controlled oscillator that can be dynamically adjusted is a voltage gain(see column 6, lines 22-24).

As to claim 7, Co discloses the circuitry wherein the setting in the divider circuit that can be dynamically adjusted is a scale factor(see column 6, lines 49-56).

As to claim 8, Co discloses the circuitry wherein the at least one control signal includes a value for the setting(see column 2, lines 11-13).

As to claim 9, Co discloses the circuitry wherein the at least one control signal is indicative of whether a value of the setting is to be increased or decreased(see column 2, lines 29-37).

As to claim 10, Co discloses the circuitry wherein the at least one control signal includes at least one data bit that corresponds to information on a value for the setting stored in a lookup table in the control circuitry(see column 4, lines 35-39).

As to claim 11, Co discloses the circuitry wherein the at least one control signal set by a programmable logic device(frequency synthesizer 1, see Fig. 6)(see column 3, lines 37-40).

As to claim 12, Co discloses the circuitry wherein the at least one control signal is set by circuitry external to the programmable logic device(see column 3, lines 37-40).

As to claim 13, Co discloses the circuitry wherein the at least one control signal is set by user input(see column 3, lines 45-46).

As to claim 18, Co discloses a programmable logic device(frequency synthesizer 1, see Fig. 6) comprising clock data recovery (CDR) circuitry(PPL 2, see Fig. 6) that receives as input a reference clock signal(signal line 10, see Fig. 6) and a CDR signal and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal, and to use the recovered clock signal to recover clock information and data information from the CDR signal. Co also discloses the programmable logic device comprising

control circuitry(phase-locked loop adjustment circuit 3, see Fig. 6) that receives as input at least one control signal and is operative to dynamically adjust a bandwidth(loop bandwidth, see column 4, line 20) of the CDR circuitry by changing a setting in at least one component in the CDR circuitry while the CDR circuitry is processing data, wherein the control circuitry is capable of changing the setting in a charge pump(charge(current) pump 400, see Fig. 3), a loop filter(loop filter 500, see Fig. 6), a voltage controlled oscillator(Variable (Voltage Controlled) Oscillator 600, see Fig. 6), and a divider circuit(output frequency divider 200, see Fig. 6) in the CDR circuitry(see column 6, lines 35-39).

As to claim 19, Co discloses the programmable logic device wherein the CDR circuitry comprises a phase frequency detector(phase detector 300, see Fig. 6) receiving as input the reference clock signal having a signal output(signal line 50, see Fig. 6), the charge pump having a pump input(signal line 50, see Fig. 6) coupled to the signal output of the phase frequency detector and having a pump output(signal line 60, see Fig. 6), and the loop filter having a filter input(signal line 60, see Fig. 6) coupled to the pump output of the charge pump and having a filter output(signal line 70, see Fig. 6). Co also discloses the voltage controlled oscillator having an oscillator input(signal line 70, see Fig. 6) coupled to the filter output of the loop filter and having an oscillator output(signal line 20, see Fig. 6), and a divider circuit having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output(signal line 40, see Fig. 6) that feeds back to the input of the phase frequency detector.

As to claim 21, Co discloses the programmable logic device wherein the setting in the at least one component comprises current in the charge pump(see column 6, lines 18-20).

As to claim 22, Co discloses the programmable logic device wherein the setting in the at least one component comprises a resistor value in the loop filter(see column 6, lines 20-22).

As to claim 23, Co discloses the programmable logic device wherein the setting in the at least one component comprises a capacitor value in the loop filter(see column 6, lines 20-22).

As to claim 24, Co discloses the programmable logic device wherein the setting in the at least one component comprises a voltage gain in the voltage controlled oscillator(see column 6, lines 22-24).

As to claim 25, Co discloses the programmable logic device wherein the setting in the at least one component comprises a scale factor in the divider circuit(see column 6, lines 49-56).

As to claim 26, Co discloses the programmable logic device wherein the at least one control signal is set by the programmable logic device)(see column 3, lines 37-40).

As to claim 27, Co discloses the programmable logic device wherein the at least one control signal is set by circuitry external to the programmable logic device(see column 3, lines 37-40).

As to claim 28, Co discloses the programmable logic device wherein the at least one control signal is set by the user input(see column 3, lines 45-46).

As to claim 29, Co discloses a programmable logic device(frequency synthesizer 1, see Fig. 6) comprising phase lock loop (PLL) circuitry(PPL 2, see Fig. 6) that receives as input a reference clock signal(signal line 10, see Fig. 6) and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal. Co further discloses the programmable logic device comprising control circuitry(phase-locked loop adjustment circuit 3, see Fig. 6) that receives as input at least one control signal and is operative to dynamically adjust a bandwidth(loop bandwidth, see column 4, line 20) of the PLL circuitry by changing a setting in at least one component in the PLL circuitry while the PLL circuitry is processing data, wherein the control circuitry is capable of changing the setting in a charge pump(charge(current) pump 400, see Fig. 3), a loop filter(loop filter 500, see Fig. 6), a voltage controlled oscillator(Variable (Voltage Controlled) Oscillator 600, see Fig. 6), and a divider circuit(output frequency divider 200, see Fig. 6) in the PPL circuitry(see column 6, lines 35-39).

As to claim 30, Co discloses the programmable logic device wherein the PLL circuitry comprises a phase frequency detector(phase detector 300, see Fig. 6) receiving as input the reference clock signal having a signal output(signal line 50, see Fig. 6), the charge pump having a pump input(signal line 50, see Fig. 6) coupled to the signal output of the phase frequency detector and having a pump output(signal line 60, see Fig. 6), and the loop filter having a filter input(signal line 60, see Fig. 6) coupled to the pump output of the charge pump and having a filter output(signal line 70, see Fig. 6). Co also discloses the voltage controlled oscillator having an oscillator input(signal

line 70, see Fig. 6) coupled to the filter output of the loop filter and having an oscillator output(signal line 20, see Fig. 6), and a divider circuit having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output(signal line 40, see Fig. 6) that feeds back to the input of the phase frequency detector.

As to claim 32, Co discloses the programmable logic device wherein the setting in the at least one component comprises current in the charge pump(see column 6, lines 18-20).

As to claim 33, Co discloses the programmable logic device wherein the setting in the at least one component comprises a resistor value in the loop filter(see column 6, lines 20-22).

As to claim 34, Co discloses the programmable logic device wherein the setting in the at least one component comprises a capacitor value in the loop filter(see column 6, lines 20-22).

As to claim 35, Co discloses the programmable logic device wherein the setting in the at least one component comprises a voltage gain in the voltage controlled oscillator(see column 6, lines 22-24).

As to claim 36, Co discloses the programmable logic device wherein the setting in the at least one component comprises a scale factor in the divider circuit(see column 6, lines 49-56).

As to claim 37, Co discloses the programmable logic device wherein the at least one control signal is set by the programmable logic device)(see column 3, lines 37-40).

As to claim 38, Co discloses the programmable logic device wherein the at least one control signal is set by circuitry external to the programmable logic device(see column 3, lines 37-40).

As to claim 39, Co discloses the programmable logic device wherein the at least one control signal is set by the user input(see column 3, lines 45-46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Co et al.(US Patent 6,803,827) further in view of Brunn et al.(US Patent 6,650,195).

As to claim 14, Co discloses a digital processing system comprising previously defined circuitry. However Co fails to disclose the previously defined circuitry coupled to processing circuitry and memory coupled to the processing circuitry.

Brunn et al teaches a digital processing system(Exemplary system 500, see Fig. 5) comprising processing circuitry(CPUs 512 and 522, see Fig. 5)) and memory(Memories 514 and 524, see Fig. 5) coupled to the processing circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Co and Brunn in order to complete the digital processing system comprising processing circuitry and memory with circuitry consisting of a phase frequency detector, charge pump, loop filter, VCO, divider circuit, and control circuitry. Motivation to do so would be to be able to dynamically adjust bandwidth within the digital processing system.

As to claim 15, Brunn discloses a printed circuit board(circuit board, see column 1, line 24) on which is mounted the previously defined apparatus.

As to claim 16, Co discloses the printed circuit board. However Co fails to disclose the printed circuit board further comprising a memory mounted on the printed circuit board and coupled to the circuitry.

Brunn teaches a memory(memories 514 and 524, see Fig. 5) mounted on the printed circuit board and coupled to the circuitry.

As to claim 17, Co discloses the printed circuit board. However, Co fails to disclose the printed circuit board comprising processing circuitry mounted on the printed circuit board and coupled to the apparatus.

Brunn teaches the processing circuitry(CPUs 512 and 524, see Fig. 5) mounted on the printed circuit board and coupled to the apparatus.

Response to Arguments

3. Applicant's arguments, filed 3/1/2006, with respect to the rejection(s) of claim(s) 1-19, 20-30, and 32-39 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Co et al.(US Patent 5,631,587).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Brown whose telephone number is (571)272-5932. The examiner can normally be reached on Monday-Friday from 7:00am to 3:30pm(EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIRS) system. Status information for the published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications are available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

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Art Unit 2116

THUAN N. DU
PRIMARY EXAMINER